Microwave Field-Effect Transistors—1976

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Abstract—**A review of recent and current work on microwave FET's and amplifiers is presented, and an extensive bibliography of recent articles is appended (250 references). First, the various FET structures (MESFET's, JFET's, and IGFET's) and their performances are reviewed. Second, the principle of operation is outlined for Si- and GaAs-MESFET's; the basic device physics, equivalent circuit, high-frequency limitations, and noise behavior are treated. Third, the design principles and performance of microwave MESFET amplifiers are summarized.**

I. Introduction

IT TOOK seventeen years from the initial introduction of the bipolar transistor in 1948 until microwave transistors with practical gain and noise figure became available. In 1965 germanium transistors invaded *L* band with noise figures under 6 dB. A milestone was reached in 1968 when the AT&T System adopted the balanced transistor amplifier, developed by Engelbrecht and Kurokawa [A1], for use in its *S*- and *C*-band microwave communication links. Since 1968 significant progress has been made in obtaining low-noise performance and high-power capability from bipolar transistors for frequencies reaching up to *X* band. At 8 GHz a silicon n-p-n transistor with 3.9-dB noise figure and 3.8-dB associated gain [A2], and a power transistor with 1-W CW output power[1] and 6-dB power gain [A3] have been reported. At 2 GHz a single (silicon) transistor chip delivers up to 30-W CW output power with 7-dB power gain and 32-percent power-added efficiency [A7]. Bipolar transistors fabricated in GaAs are still in an early stage of development [A8]–[A10].

By 1971, however, breakthroughs had been made in the development of field-effect transistors. Today, GaAs *met*al *s*emiconductor *f*ield-*e*ffect *t*ransistors (MESFET's) have higher gain, higher power-amplification efficiency, and lower noise figure than bipolar transistors above 4 GHz. More significant is the fact that FET's promise a great deal of potential for further advances. Substantial progress can be expected in the near future because of the following.

1) A large variety of FET structures (MESFET, JFET, IGFET) are suitable for microwave amplification and power generation, and some promising candidates are only in an early stage of development.

2) A variety of semiconductor materials (GaAs, InP, $In_xGa_{1-x}As$, $InAs_xP_{1-x}$) with majority-carrier transport properties[2] superior to silicon are competing for application in FET's [F5].

3) Further miniaturization to submicron dimensions can be realized in most FET structures.

4) Monolithic integration of circuits on semi-insulating substrates enables device isolation with low parasitic capacitances, low-loss interconnections, and high packing density.

This paper reviews recent and current developments in high-frequency FET's and FET amplifiers.[3] In Section II the various microwave FET structures are discussed, and their performance characteristics are summarized. Section III gives an introduction to the device physics, the small-signal characteristics, and the noise behavior of MESFET's. In Section IV the design principles and the performance of microwave amplifiers are reviewed. An extensive bibliography of recent articles is appended. Because of limited space, topics such as fabrication, packaging, reliability, oscillators, mixers, modulators, and digital applications are not treated here.

II. Microwave FET Structures and their Performance

Today MESFET's, p-n junction FET's (JFET's), and insulated-gate FET's (IGFET's) are used at microwave frequencies [B2]. The cross sections of the various FET structures are illustrated in Fig. 1. Their performance characteristics are tabulated in Table I. Fig. 1 serves as a guide for the following discussion; i.e., first the MESFET's, then the JFET's, and finally the IGFET's are described.

A. MESFET

In 1969 Middelhoek realized a silicon MESFET with 1-μm gate length by projection masking [X1], [X2]. This FET had a 12-GHz maximum frequency of oscillation [C1] which was considerably higher than for previously known FET's and comparable to f_{max} of the best bipolar transistors at that time. The next significant step was the fabrication of 1-μm MESFET's on GaAs. As a result, FET's with f_{max} of 50 GHz and useful gain up to 18 GHz became available in 1971 [C2]–[C6]. This substantial improvement in device performance is due to the following reasons. 1) in GaAs the conduction electrons have a six times larger mobility and a two times larger peak drift velocity than in silicon [F1]. Therefore, parasitic resistances are smaller, the transconductance is larger, and the transit time of electrons in the high-field region is shorter. 2) The active layer is grown on a semi-insulating GaAs substrate with resistivity larger than $10^7\ \Omega\cdot$cm. The large parasitic capacitance of the gate bonding pad can thus be eliminated by positioning the pad on the substrate.

In 1972 it became apparent that GaAs-MESFET's are capable of very low-noise amplification [C4]–[C6]. Liechti

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[1] Combined power from two chips.

[2] Minority-carrier lifetime and mobility are of no concern in unipolar transistors. Therefore, materials with optimized transport properties for electrons but poor performance for holes can be chosen.

[3] The reader is also referred to a review paper on the same topic by Turner [B1].

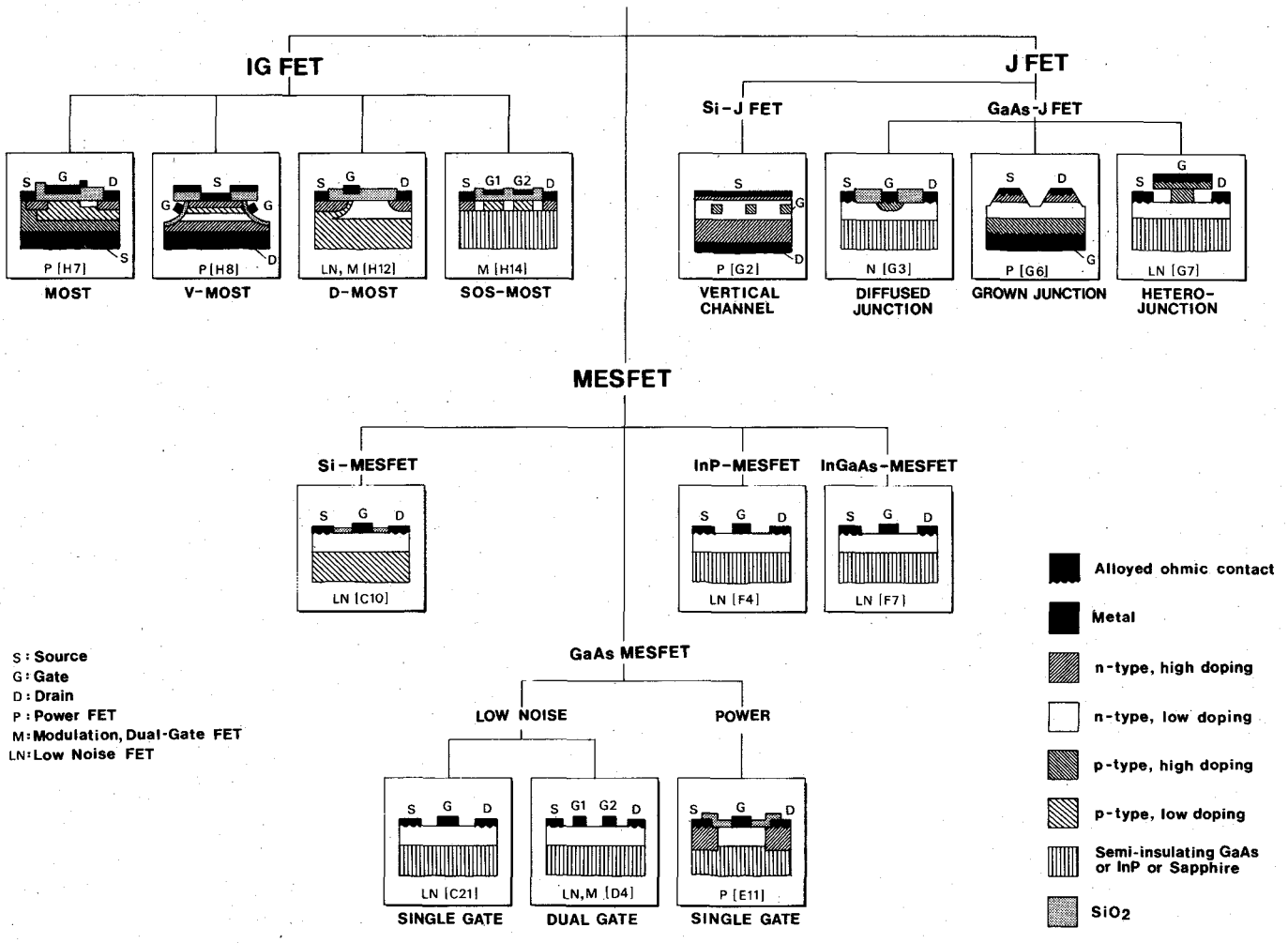

Fig. 1. This "family tree" of microwave FET's shows the cross sections of the various FET structures. Their performance characteristics are listed in Table I.

TABLE I
PERFORMANCE DATA OF THE MICROWAVE FET STRUCTURE SHOWN IN FIG. 1

Type*	Semi-conductor	Single/ Dual Gate	Channel Type	Channel Length (μm)	Channel Width (mm)	Appli-cation*	Fre-quency (GHz)	Output Power CW (W)	Assoc. Power Gain (dB)	Small Signal Gain (dB)	Power** Added Effic. (%)	Noise Figure (dB)	Assoc. Gain (dB)	Casc. Noise Figure† (dB)	Max. Avail. Gain (dB)	Reference
MESFET																
Silicon	Si	SG	n	0.5		LN	10					5.8			5.9	[C10]
LN SG GaAs	GaAs	SG	n	0.5		LN	10					2.7	10.5	3.1	13	[C21]
LN SG GaAs	GaAs	SG	n	1		LN	10					3.2	8.0	3.6	10	[D4]
LN DG GaAs	GaAS	DG	n	1		LN,M	10					4.0	12	4.2	18	[D4]
P SG GaAs	GaAs	SG	n	1.5	5.2	P	8	2.2	3.2	4.2	22					[E11]
P SG GaAs	GaAs	SG	n	1.2	0.6	P	22	0.14	4.8	5.6	9					[E17]
LN SG InP	InP	SG	n	1		LN	10					4.7	6.6	5.4	7.8	[F4]
LN SG InGaAs	InGaAs	SG	n	1		LN	7					5.7	5.0	7.0	18	[F7]
JFET																
Silicon	Si	SG	n	1	1.8	P	2.7	0.2	6.0		19					[G2]
Diff. Junction	GaAs	SG	n	2		LN	4					2.5	10	2.7	10	[G3]
Grown Junction	GaAs	SG	n	1.5	6.1	P	6	1.0	6.0	7.0	26					[G6]
Heterojunction	GaAs	SG	n	2		LN										[G7]
IGFET																
MOST	Si	SG	n	5	20	P	0.7	16	6	10	26					[H7]
V-MOST	Si	SG	n	1	18	P	2	4.0	5	6	32					[H9]
SG D-MOST	Si	SG	n	1		LN	1					3.0	9.0	3.3	-	[H13]
DG D-MOST	Si	DG	n	1		LN,M	1					4.5	14	4.6	15	[H13]
DG SOS-MOST	Si	DG	n	4		M	0.5								25	[H14]

* LN - low noise amplification; P - power amplification; M - modulation, switching or amplification with controlled gain; SG - single-gate FET; DG - dual-gate FET.

** The power added efficiency is defined as the RF output power minus the RF input power divided by the dissipated dc power.

† The cascaded noise figure is defined by Eq. (15).

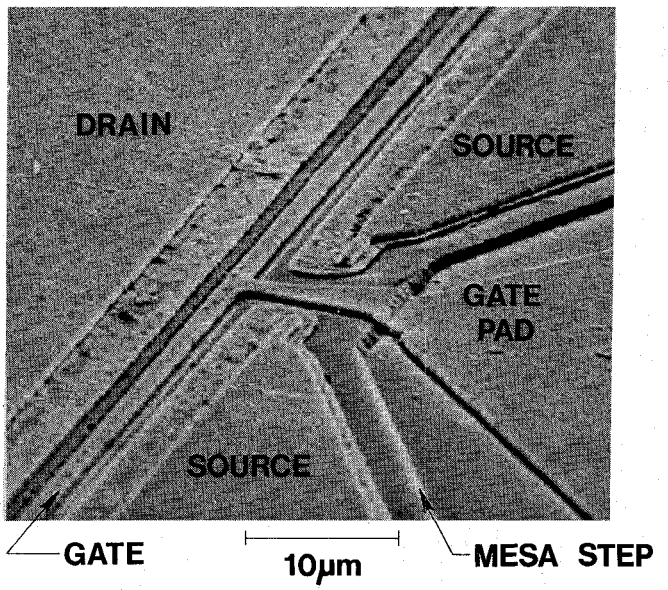

Fig. 2. This scanning electron micrograph shows the center section of a low-noise MESFET. The source and drain are alloyed ohmic contacts to the underlying conductive layer. The gate is the narrow metal stripe forming a Schottky contact. The width of the depletion layer under the gate controls the current flowing from drain to source. To the right, the gate metal runs over a mesa step (edge of the conductive layer) and widens on the semi-insulating substrate into a large bonding pad.

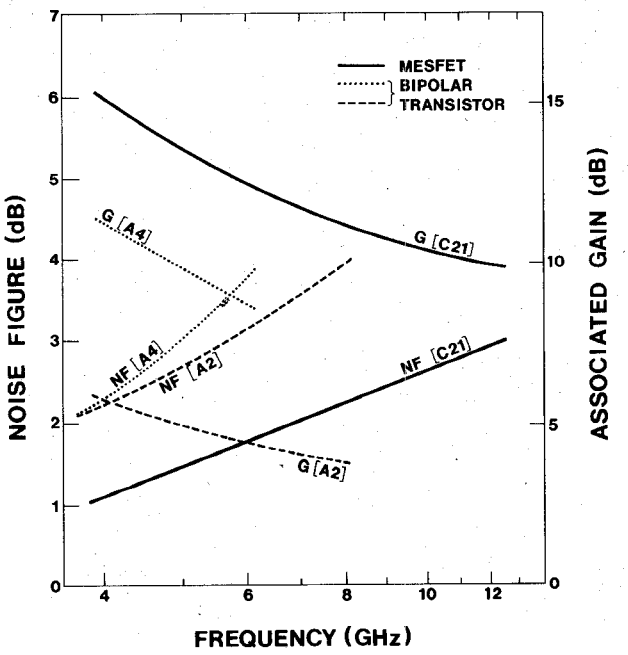

Fig. 3. Lowest reported noise figures and associated gains of microwave transistors are plotted versus frequency. The GaAs-MESFET reported by Ogawa *et al.* [C21] has 0.5-μm gate length. The dashed line represents the Si bipolar transistor with the lowest published noise figure [A2]. The bipolar transistor with the dotted line [A4] has a considerably higher gain.

et al. [C5] reported a noise figure of 3.5 dB with 6.6-dB associated gain at 10 GHz. Baechtold [M7], [M8] proposed a noise model that agrees well with measurements taking carrier velocity saturation and intervalley scattering into account. In the past few years, small-signal GaAs-MESFET's have been fabricated and characterized by various laboratories [C7]–[C28]. A scanning-electron micrograph of a typical low-noise MESFET is shown in Fig. 2. Lowest reported noise figures and associated gains are plotted in Fig. 3 versus frequency. Best noise performance is achieved with 1) a high-purity buffer layer between the substrate and the active layer [C26]; 2) a high doping level in the active n-layer (2.5×10^{17} cm^{-3} [C21]); 3) smallest possible source and gate-metal resistance [C21], [C22]; and 4) short gate length (0.5 μm [C10], [C21]).

A MESFET structure with two gates is shown schematically

in Fig. 1. This FET has a higher gain and a lower feedback capacitance than the single-gate counterpart [C21], [D1]–[D7]. In addition, the gain can be controlled over a wide range (44 dB [D4]) by varying the dc bias of the second gate. This feature can be used for automatic gain control in amplifiers [D6]. The gain modulation response is very fast. Pulse-amplitude modulation of an RF carrier with less than 100-ps fall and rise times has been demonstrated [D3], [D4].

The GaAs-MESFET is not limited to small-signal low-noise applications. The first power MESFET's appeared in 1973 and were of planar construction as shown in Fig. 4. Fukuta *et al.* [E1] designed a MESFET with 20 gates, each 1 μm long and 400 μm wide, operated in parallel and interconnected with a second metallization layer. At 2 GHz this MESFET exhibited 1.6-W output power[4] with 5-dB power gain and 21-percent power-added efficiency. At the same time, Napoli *et al.* [E2] presented a power transistor with self-aligned[5] gates [Fig. 4(c)]. Multiple gate, source, and drain pads had to be interconnected with bonding wires. The planar power FET has been further developed by various laboratories [E3]–[E19]. The techniques yielding high-power capability per unit gate width are:

1) the use of a high-resistivity epitaxial buffer layer to isolate the active layer from the bulk-grown substrate [E16];
2) the addition of inlaid n^+-regions under the source and drain electrodes, shown in Fig. 4(b), to increase the drain-source breakdown voltage and decrease the parasitic contact resistances [E11];
3) the design of short gate branches to prevent current crowding and to lower the gate-metal resistance [E11];
4) the flip-chip mounting of the transistor to decrease the thermal resistance and the source-to-ground lead inductance [E7], [E15].

A photomicrograph of a power MESFET from Fujitsu Laboratories [E9] with 104 gate branches, each 1.5 μm long and 50 μm wide, is shown in Fig. 5. Recently reported performance data of power MESFET's are summarized in Table II. The output powers from single chips, operated CW Class A, range from 4 W at 4 GHz to 0.14 W at 22 GHz and power-added efficiencies vary between 44 and 9 percent. Highest efficiency has been obtained by Huang *et al.* [E18] in Class B operation; 68 percent at 4 GHz and 41 percent at 8 GHz have been measured. These are the highest reported efficiencies of all microwave solid-state devices in this frequency range. The performance figure of merit M_F proposed by Drukier *et al.* [E15] is also listed in Table II. M_F measures the added RF power per unit gate width times the square of the operating frequency. The MESFET with the largest M_F delivers 140-mW output power with 4.8-dB power gain and 9-percent power-added efficiency at 22 GHz [E17].

A new device with better heat-sink properties has been proposed by Blocker *et al.* [E5] for power MESFET's.[6] The metallization layout and the cross section of this MESFET are

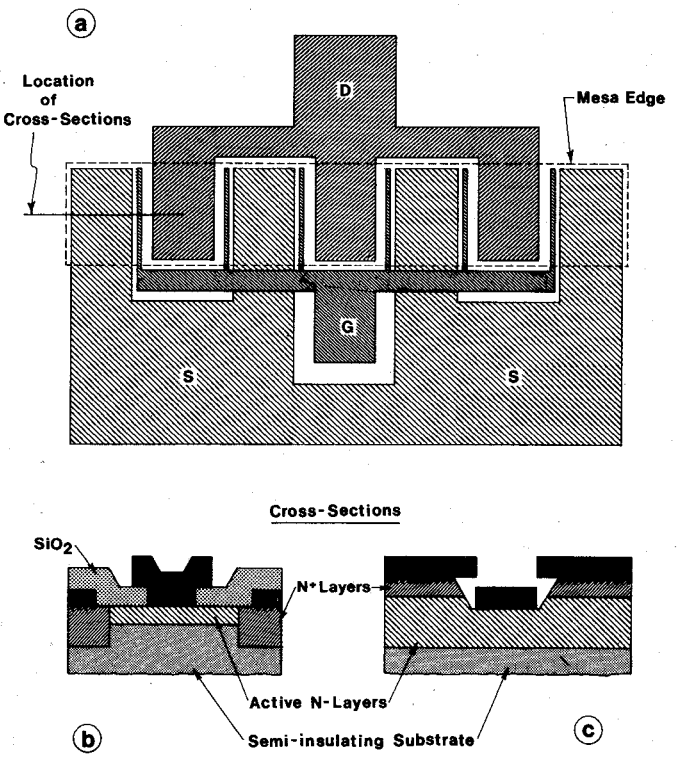

Fig. 4. (a) Illustrates schematically the metallization layout of the planar power MESFET shown in Fig. 5. The gate branches are interconnected with a metal line that crosses over the source. Multigate MESFET's with cross sections (b) [E11] and (c) [E1], [E12]–[E18] have been realized.

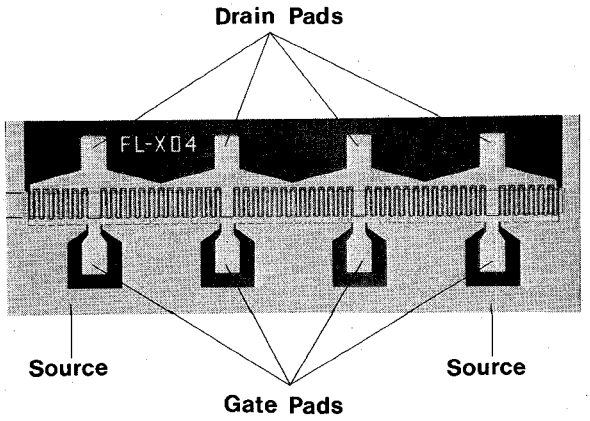

Fig. 5. This photomicrograph shows a power MESFET with 104 gate branches, each 1.5 μm long and 50 μm wide, connected in parallel. The chip delivers 0.9-W output power with 6-dB power gain and 30-percent power-added efficiency at 6 GHz [E9]. (Courtesy of M. Fukuta, Fujitsu Laboratories.)

[4] Measured at 1-dB gain compression.

[5] The location of the gates between the source and drain edges is defined by a fabrication method which does not require a critical realignment step.

[6] A similar structure has been realized by Vergnolle *et al.* [G6] in the form of a GaAs p-n junction FET (see below).

TABLE II
PERFORMANCE OF EXPERIMENTAL MICROWAVE POWER TRANSISTORS
CW DATA OF SINGLE-CHIP GaAs-MESFET's,[1] GaAs-JFET's,[2] AND Si BIPOLAR TRANSISTORS[3]

Frequency (GHz)	Transistor Type	Output Power (W)	Power Gain[4] (dB)	Small-Signal Gain[5] (dB)	Power Added Efficiency[6] (%)	Figure of Merit[7] (WGHz²/mm)	Gate Length[8] (μm)	Total Gate Width[9] (mm)	Number of Cells on Chip	Operating Conditions (Class A,B,C)	Company [Reference]
2.0	*Bipolar*	*30*	*7.0*	-	*32*	*2.2*	*1.5*	*43*	*10*	*C*	*MSC [A7]*
4.0	*Bipolar*	*8.0*	*7.0*	-	*25*	*4.3*	*1.0*	*24*	*8*	*C*	*TRW [A6]*
	MESFET	4.0	6.0	7.0	44	9.2	1.5	5.2	2	A	Fujitsu [E11]
6.0	*Bipolar*	*1.5*	*4.4*	-	*23*	*11*	*1.5*	*3.1*	*4*	*C*	*Hewlett-Packard [A5]*
	JFET	1.0	6.0	7.0	26	4.4	1.5	6.1	2	A	Thomson-CSF [G6]
	MESFET	2.7	5.0	6.0	31	13	1.5	5.2	2	A	Fujitsu [E11]
8.0	*Bipolar*	*0.5*	*6.0*	-	*22*	*22*	*0.5*	*1.1*	*2*	*B*	*Texas Instruments [A3]*
	MESFET	0.6	6.0	7.5	34	21	1.5	1.4	3	A	Plessey [E19]
	MESFET	2.2	3.2	4.2	22	14	1.5	5.2	2	A	Fujitsu [E11]
15.0	MESFET	0.45	5.2	6.7	13	59	1.5	1.2	2	A	RCA [E17]
22.0	MESFET	0.14	4.8	5.6	9	76	1.5	0.6	1	A	RCA [E17]

[1]Operated with common source.
[2]Operated with common gate.
[3]Operated with common base.
[4]Associated with the stated output power.
[5]Only applicable for Class A operation.
[6]Defined as RF output power minus RF input power divided by the dissipated dc power.
[7]Defined as added RF power x (frequency)² divided by the total gate width or emitter periphery.
[8]Or emitter finger width.
[9]Or total emitter periphery.

shown in Fig. 6. Interdigitated source and drain fingers are located on the top side of the chip, and the gate with plated heat sink is located on the bottom side. The channel is confined to an area within the constricted cross section in the n-layer. This structure has the following advantages: 1) it places the active region in intimate thermal contact with the heat sink; 2) it enables an interdigitated structure without overcrossing, since the ohmic contacts and the gate are located on different sides of the chip; 3) it reduces the parasitic source-to-gate resistance; and 4) it makes a self-aligned process possible. Disadvantages are the higher gate-to-drain and gate-to-source capacitances.

Besides Si and GaAs, InP has been investigated for application in MESFET's. InP has a 50-percent higher maximum drift velocity than GaAs[7] [F2], [F3]. Therefore, one expects a higher current-gain bandwidth f_T for InP-MESFET's. Barrera and Archer [F4] have measured an f_T that is 1.6 times larger than in analogous GaAs devices. However, the maximum frequency of oscillation, f_{max}, is 20 percent lower. Degenerate feedback resulting from a large gate-to-drain capacitance and a small output resistance degrades the gain performance. Noise figures of InP-MESFET's are slightly higher.

The ideal semiconductor for FET's has simultaneously a large mobility, large maximum drift velocity, and large avalanche breakdown field. Consequently, a small electron effective mass, a large intervalley separation, and a large energy gap are required. The first and last requirements are conflicting, since a large energy gap implies a large effective mass; but it is possible to design a better compromise than is found in the binary compounds GaAs and InP.

[7] The low field mobility of InP is 25 percent lower, however.

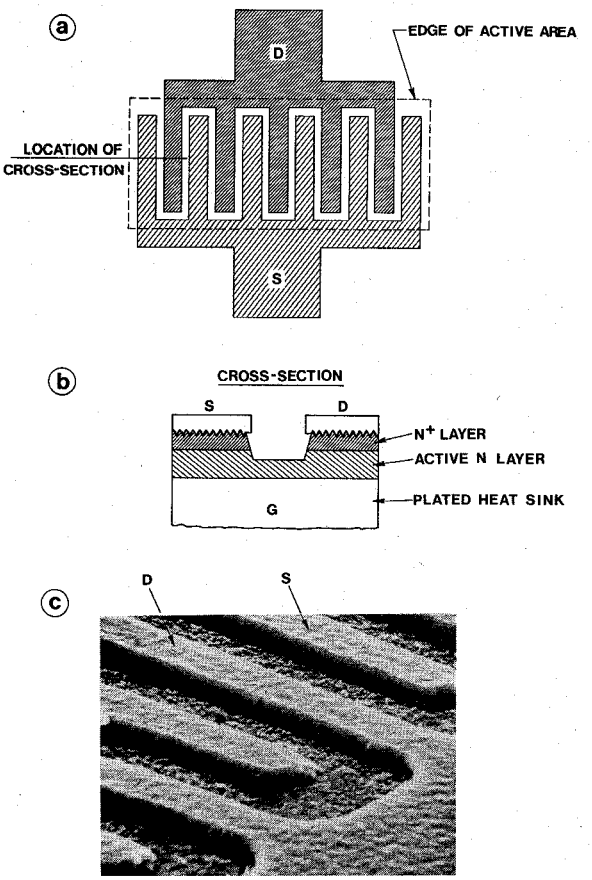

Fig. 6. Power MESFET structure with plated heat sink on the gate as proposed in [E5]. (a) Shows the metallization on the top side of the chip with interdigital source and drain fingers. Outside the active area, the GaAs is converted into semi-insulating material by proton bombardment. (b) Shows the cross section of the device with the source and drain on top and the gate with plated heat sink on the bottom of the chip. (c) Shows the top view of the FET chip [G6]. (SEM courtesy of C. Vergnolle, Thomson-CSF.)

Two systems which merit consideration are the mixed crystals InAs–InP and InAs–GaAs [F5], [F6]. Decker *et al.* [F7] have grown thin films of $In_{0.04}Ga_{0.96}As$ directly on GaAs. MESFET's fabricated on this material are very similar to their GaAs counterpart with the exception of a larger output resistance. The step in the bandgap at the InGaAs–GaAs interface constrains the electrons to the InGaAs layer and prevents penetration of hot electrons into the substrate at the high-field channel region.

B. JFET

A great deal of effort has been spent on developing p-n junction FET's for microwave applications. In the past, JFET's have not moved to higher frequencies as rapidly as MESFET's primarily because of the difficulty in realizing closely defined p-conducting regions by diffusion or implantation.[8] In more recent developments, such as the power JFET with ion-milled channel [G6] or the heterojunction JFET [G7], these limitations do not apply and rapid advances can be expected.

In 1972 Teszner [G1] described an Si-JFET with a vertical channel for power amplification. This multielement transistor has buried p^+-gate fingers, and the ohmic contacts for source and drain are located on opposite sides of the chip (Fig. 1). The structure was later realized by high-energy ion implantation of the gate [G2]. In this vertical geometry, no implantation-induced defects are generated in the channel. Consequently, low annealing temperatures were used and patterns with 1-μm-long channels were realized. Test devices, with 1.8-mm total gate width, delivered 200-mW output power with 6-dB power gain at 2.7 GHz.

In GaAs, Zuleeg *et al.* [G3] have realized a low-noise JFET with a diffused p-n junction of 2-μm length. The transistor exhibits 2.5-dB noise figure and 10-dB associated gain at 4 GHz. This JFET has a high tolerance to fast neutron radiation. A 1-MeV neutron fluence of 5×10^{16} neutrons/cm^2 is required to degrade the transconductance by 10 percent [G4], [G5].

A power GaAs-JFET has been built by Vergnolle *et al.* [G6] [Fig. 6(c)]. The construction is similar to the one shown in Fig. 6(b), except that the Schottky barrier is replaced by a p-n junction grown on a p^+-substrate. This structure has the same advantages as the MESFET of Fig. 6(a) and (b), except that the thermal resistance is limited by the spreading resistance in the GaAs substrate. This JFET with 1.5-μm gate length and 6-mm total gate width delivers 1-W output power[9] with 6-dB power gain and 26-percent power-added efficiency at 6 GHz.

A low-noise FET with a heterojunction gate is now under development at Matsushita Electric [G7]. The junction consists of a p-type $Ga_{0.5}Al_{0.5}As$ layer grown on top of an n-type GaAs layer. The p-layer can be selectively etched to the shape of a 1-μm gate strip. This feature combined with a self-aligned process enables simple fabrication of GaAs-JFET's.

C. IGFET

Field-effect transistors with insulated gates are of interest for power amplification. They offer the following advantages over MESFET's or JFET's. 1) In the active region of an enhancement-mode MOSFET, the input capacitance and the transconductance are almost independent of gate voltage, and the output capacitance is independent of the drain voltage.[10] This leads to very linear (Class A) power amplification with low amplitude and phase distortion. 2) The active gate-voltage range can be larger because n-channel depletion-type IGFET's can be operated from the depletion-mode region ($-V_{GS}$) to the enhancement-mode region ($+V_{GS}$). Unfortunately, practical IGFET's have only been made on Si. Attempts to realize a usable device in GaAs have had only limited success [H1], [H2]. It is difficult to fabricate an insulating film which produces an interface to n-GaAs with a low density of electron states [H2]–[H4]. Recent advances with anodic native oxides of GaAs show promising interface and dielectric properties [H5]. A density of fast interface states of 1 to 2×10^{11} cm^{-2}eV^{-1} has been observed. This is still 10 times higher than the best results in Si [H6], but sufficiently low for MOSFET operation.

Morita *et al.* [H7] have developed an n-channel depletion-type Si-MOSFET which delivers 16-W output power[11] with 6-dB associated power gain and 26-percent power-added efficiency at 700 MHz. The device has a conventional planar structure with diffused n^+ drain and source regions and a 5-μm-long and 20-mm-wide channel. A very different approach is the vertical-gate MOS transistor (VMOST) designed for power amplification [H8]. This device consists of mesa strips with control gates on both sides of each strip (Fig. 1). The source contact is made to the top surface of the mesa, and the n^+-substrate acts as a common drain. The length of the vertical n-channel is controlled by epitaxial growth and the metal-gate length by angular metal deposition. For a 1-μm-long and 18-mm-wide channel, a CW output power of 4 W[12] with 5-dB power gain has been measured at 2 GHz by Heng [H9]. Also, a double-diffused MOSFET (D-MOST) can be fabricated with channel lengths of less than 1 μm using standard photolithography [H10]. The short channel results from subsequent diffusions of the channel and source impurities under the same oxide layer. This technique gives accurate control of the channel length comparable to the control over the base width in diffused bipolar transistors. The D-MOST has been developed for low-noise UHF amplification by Sigg *et al.*

[8] Lateral diffusion or lateral spreading of the ions during implantation and during the subsequent high-temperature annealing step widen the p-regions with respect to mask dimensions.

[9] Measured at 1-dB gain compression. For a performance comparison with MESFET's, see Table II.

[10] This applies to MOSFET's with n^- drift region.

[11] Measured at 4-dB gain compression.

[12] Measured at 1-dB gain compression.

[H11], [H12]. Single-gate FET's exhibit 3.0-dB noise figure and 9.0-dB associated gain at 1 GHz [H13]. Dual-gate FET's suitable for mixers and for amplifiers with automatic gain control have 4.5-dB noise figure with 14-dB gain [H13]. Silicon-on-sapphire MOS transistors (SOS-MOST) have also been developed for UHF applications with the advantage of very low drain-to-channel and drain-to-source capacitances. A small-signal dual-gate SOS-MOST has been built by Ronen and Strauss [H14] with a 4-μm channel length yielding 25-dB gain at 0.5 GHz.

D. Conclusion

The MESFET's have been the most successful among the microwave FET's in low noise and in power amplification above 2 GHz. The reasons for this are easy realization on GaAs and the fact that the two critical dimensions, the gate length and channel thickness, can be accurately controlled. With advanced fabrication processes, such as E-beam lithography [C3], [C17], ion implantation [C13], [C16], [C27], [W4], [X4], and molecular-beam epitaxy [C28], further improvement in dimensional control is obtained. In comparison with silicon bipolar transistors, MESFET's have higher maximum frequency of oscillation, lower noise figures, and larger associated gain at microwave frequencies (Fig. 3). They also have higher reverse isolation and lower third-order intermodulation distortion. Above 4 GHz, GaAs MESFET's have better efficiency as power amplifiers than bipolar transistors (Table II). In addition, FET's do not exhibit secondary breakdown, are self-ballasting,[13] and have inherently higher input impedance. Also, the gate-to-source and drain-to-source impedances are fairly insensitive to temperature variations [S6]. As majority-carrier devices, FET's are more immune to the effects of neutron and gamma radiation than bipolar transistors [G4], [G5], [Q13]. Currently, much effort is spent in determining the reliability, failure modes, and stability of GaAs MESFET's [I1]–[I9]. Preliminary results indicate a meantime to failure in excess of 10^7 h at 70°C channel temperature as reported by Irie *et al.* [I3] and Abbott and Turner [I5]. Ch'en *et al.* [I7], [I8] observed an improvement in the long-term stability of MESFET parameters after passivating the GaAs surface with a thin coating of polycrystalline GaAs.

III. MESFET Principle of Operation

In this section, the physical principles in the operation of a silicon MESFET are explained. Then the differences between silicon and GaAs-MESFET's are outlined and effects occurring in FET's with very short gate length are discussed. Next, the equivalent circuit is presented and high-frequency limitations are described. Finally, the principles of the noise behavior are presented.

[13] With rising temperature, the channel and source resistances increase, preventing "thermal runaway."

A. Principles of Silicon MESFET Operation

The current-voltage characteristic of a thin n-type silicon layer in which electrons are carrying the current is plotted in Fig. 7(a). This layer is supported by an insulating silicon substrate. At the surface of the conducting layer, two ohmic contacts are made, called the source and drain. A cross section of this device is shown in Fig. 7(a).[14] If a positive voltage V_{DS} is applied to the drain, electrons will flow from source to drain. Hence the source acts as the origin of carriers and the drain as a sink. For small voltages, the silicon layer behaves like a linear resistor. For larger voltages, the electron drift velocity does not increase at the same rate as the electric field E (Fig. 8). As a result, the current-voltage characteristic falls below the initial resistor line. As V_{DS} is further increased, E reaches a critical field, E_c,[15] for which the electrons reach a maximum velocity, v_s (Fig. 8). At this drain voltage, the current starts to saturate.

In Fig. 7(b) a metal-to-semiconductor contact, called the gate, has been added between source and drain. This contact creates a layer in the semiconductor that is completely depleted of free-carrier electrons. This depletion layer acts like an insulating region and constricts the cross section available for current flow in the n-layer. The width of the depletion region depends on the voltage applied between the semiconductor and the gate. In Fig. 7(b) the gate is shorted to the source and a small drain voltage is applied. Under these conditions, the depletion layer has a finite width and the conductive channel beneath has a smaller cross section d than in Fig. 7(a). Consequently, the resistance between source and drain is larger, as shown in Fig. 7(b). The current I_{DS} flowing from drain to source is given by

$$I_{DS} = wqn(x)v(x)d(x) \tag{1}$$

where w is the gate width (see Fig. 11), q the charge of an electron, n the density of conduction electrons, v their drift velocity, d the conductive layer thickness, and x the coordinate in the direction of the electron drift. The electron density n is equal to the constant donor density N_D as long as the field does not exceed the critical value E_c. The voltage along the channel increases from zero at the source to V_{DS} at the drain. Thus the metal-to-semiconductor junction becomes increasingly reverse biased, and the depletion layer becomes wider as we proceed from source to drain. The resulting decrease in conductive cross section d must be compensated by an increase of electric field and electron velocity v to maintain a constant current through the channel. As the drain voltage is increased further, the electrons reach the maximum limiting velocity v_s under the drain end of the gate. This is illustrated in Fig. 7(c). The channel is constricted to the smallest cross section d_0 under the gate

[14] For simplicity, the bending of the bands at the free surface of the n-layer and the depleted region at the substrate interface are neglected. Also the electric field is assumed to be uniform in the n-region between the contacts.

[15] In silicon, the value of E_c cannot be accurately defined.

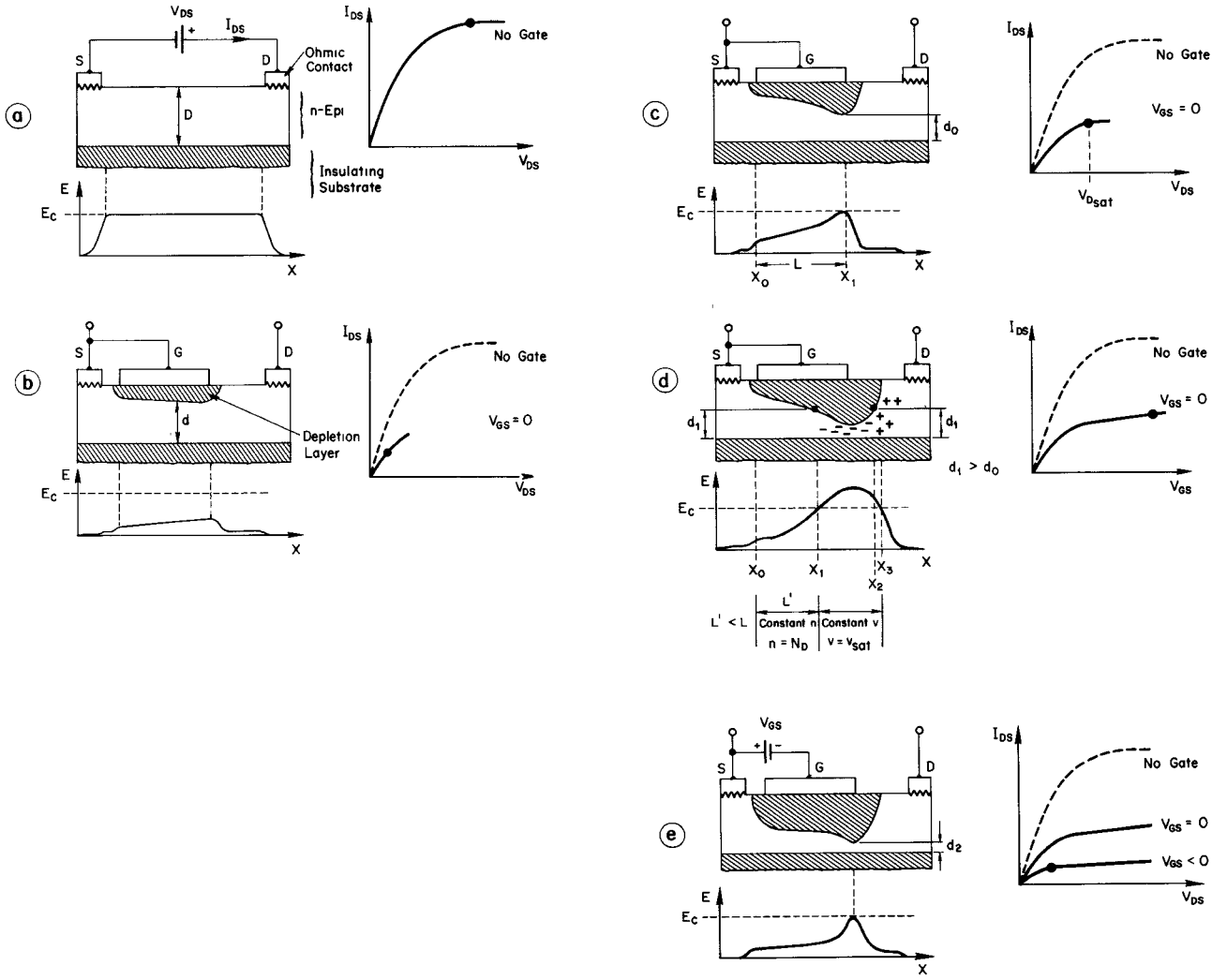

Fig. 7. (a) Shows the I–V characteristic of an n-type silicon layer with two ohmic contacts. The current saturates because the electrons reach a maximum drift velocity at the critical field E_c. In (b)–(d), the current is controlled by the depletion layer under a Schottky gate, shorted to the source. In (c) the current starts to saturate at $V_{D_{sat}}$, and (d) shows the formation of a stationary dipole layer in the channel for $V_{DS} > V_{D_{sat}}$ [J12], [K1]. (e) Illustrates the condition for a negative gate bias. The depletion layer is wider, it constricts the conductive cross section further, and causes the current to saturate at a lower level.

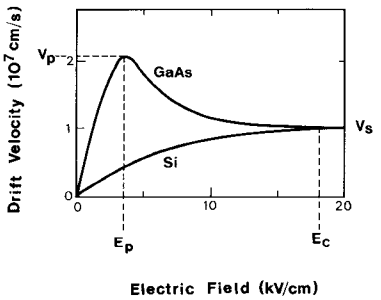

Fig. 8. Equilibrium electron drift velocity versus electric field in GaAs and silicon (after Ruch [K11]).

edge, the electric field reaches the critical value at this point, and the current starts to saturate.

If the drain voltage is increased beyond $V_{D_{sat}}$, the depletion region widens toward the drain. The point x_1, where the electrons reach the limiting velocity, moves slightly toward the source [Fig. 7(d)]. As x_1 moves closer to the source, the voltage at x_1 decreases.[16] Consequently, the conductive cross section d_1 widens and more current is injected into the velocity-limited region. This results in a positive slope of the I_{DS} curve and a finite drain-to-source resistance beyond current saturation [J8], [J12]. The effect is particularly pronounced in microwave MESFET's with short gate lengths.

Proceeding from x_1 toward the drain, the channel potential increases, the depletion layer widens, and the channel cross section d becomes narrower than d_1. Since the electron velocity is saturated, the change in channel width must be compensated for by a change in carrier concentration to maintain constant current. According to (1), an electron accumulation layer forms between x_1 and x_2, where d is smaller than d_1. At x_2 the channel cross section is again d_1 and the negative space charge changes to a positive space charge to preserve constant current. The

[16] The average field between x_0 and x_1 remains nearly unchanged while the distance between x_0 and x_1 decreases.

positive space charge is caused by partial electron depletion. The electron velocity remains saturated between x_2 and x_3 due to the field added by the negative space charge. In short, the drain voltage applied in excess of $V_{D_{sat}}$ forms a dipole layer in a channel that extends beyond the drain end of the gate [J12], [K1].

When a negative voltage is applied to the gate [Fig. 7(e)], the gate-to-channel junction is reverse biased, and the depletion region grows wider. For small values of V_{DS}, the channel will act as a linear resistor, but its resistance will be larger due to a narrower cross section available for current flow. As V_{DS} is increased, the critical field is reached at a lower drain current than in the $V_{GS} = 0$ case, due to the larger channel resistance. For a further increase in V_{DS}, the current remains saturated. In essence, the MESFET consists of a semiconducting channel whose thickness can be varied by widening the depletion region under the metal-to-semiconductor junction. The depletion region widening is the effect of a field or voltage applied between gate and channel of the transistor.

Various analytical solutions for the voltage-current characteristics of short-gate MESFET's with field-dependent electron velocity have been developed. The majority [J2]–[J7] follow a one-dimensional analysis based on the gradual-channel approximation proposed by Shockley [J1]. They compute the drain current at the onset of current saturation [Fig. 7(c)]. Two-dimensional approximations of the field distribution for large drain voltages have also been derived [J8]–[J12]. These analytical solutions make allowance for space charges in the channel and enable calculations of the small-signal drain-to-source resistance in the saturated current region. Much effort has also been concentrated on accurate two-dimensional numerical solutions for Si [K1]–[K7], for GaAs and InP [K8]–[K14].

B. Principles of Gallium Arsenide MESFET Operation

In GaAs, the analysis in the high-field region is considerably more complicated than in Si because 1) the equilibrium electron velocity versus electric field reaches a peak value at about 3 kV/cm, then decreases and levels off at a saturated velocity that is about equal to the limiting velocity in silicon (Fig. 8) [F1], [K11]; 2) for gate lengths shorter than 3 μm, a nonequilibrium velocity-field characteristic has to be considered [K13].

A rigorous treatment of the electron transport in GaAs-MESFET's, based on the equilibrium velocity-field characteristic, has been carried out by Himsworth [K9]. Fig. 9 summarizes the key features of a transistor with 3-μm gate length operated far in the saturated current region. The narrowest channel cross section is located under the drain end of the gate. The drift velocity rises to a peak at x_1, close to the center of the channel, and falls to the low saturated value under the gate edge. To preserve current continuity according to (1), heavy electron accumulation has to form in this region because the channel cross section is narrowing and, in addition, the electrons are moving progressively slower with increasing x. Exactly the opposite occurs between x_2 and x_3. The channel widens and the

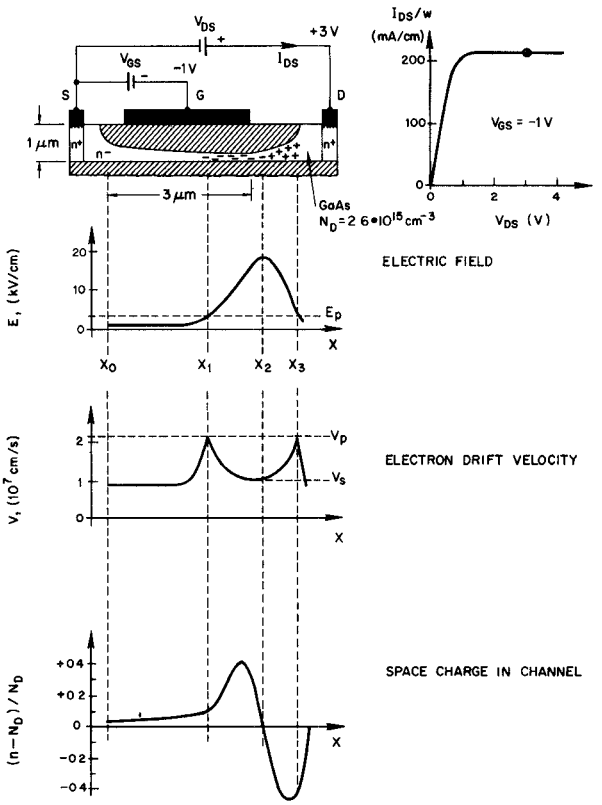

Fig. 9. The channel cross section, electric field, electron drift velocity, and space-charge distribution in the channel are illustrated for a GaAs-MESFET operated in the current-saturated region (data from Himsworth [K9]). Proceeding from x_1 to x_2, the channel cross section becomes narrower and, in addition, the electrons "slow down." To preserve current continuity, a heavy electron accumulation has to form. The opposite occurs between x_2 and x_3.

electrons move faster causing a strong depletion layer.[17] The charges in the accumulation and depletion layers are nearly equal and most of the drain voltage drops in this stationary dipole-layer.

In microwave FET's with very short gate length, the electrons do not reach equilibrium transport conditions in the high-field region of the channel. Nonequilibrium velocity-field characteristics in GaAs have been studied by computer simulations using Monte Carlo methods [K11]–[K14]. In a simplified approach, slow electrons are injected into a constant-field region and their drift velocity is monitored [K11]–[K13]. The situation is schematically illustrated in Fig. 10. As long as E is below the threshold field E_p, the electrons remain in equilibrium conditions. If the electrons enter a high-field region ($E > E_p$), they are accelerated to a higher velocity before relaxing to the equilibrium velocity.[18] This overshoot to more than twice the

[17] This region is not fully depleted of free electrons in contrast to the cross-hatched depletion layers.

[18] For $E < E_p$, electrons remain in the "lower valley" where they have a high mobility. For $E \gg E_p$, almost all electrons are transferred to a "satellite valley," a state in which they have a low mobility; i.e., low velocity at a given field. If the field changes suddenly from a value below to above E_p, a time period of approximately 1 ps passes before the carriers are transferred from the lower to the upper valley. During this time, the electrons remain in the high-mobility state in which they can acquire a high velocity in the high field.

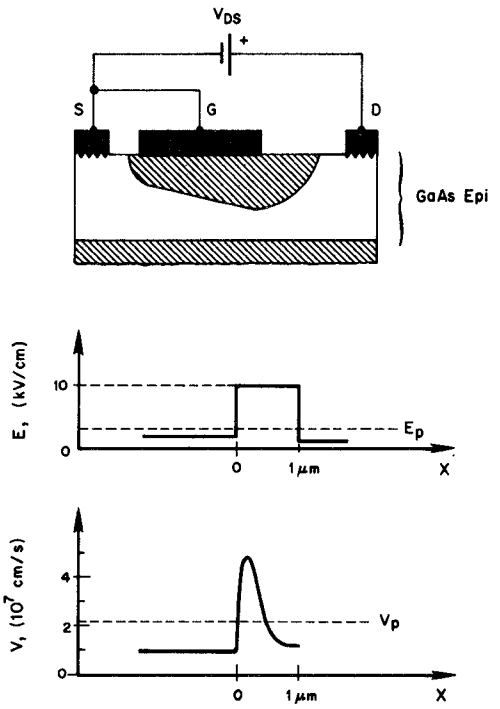

Fig. 10. This figure shows schematically the velocity overshoot of electrons as they enter the high-field region ($E > E_p$) under the gate (data from Ruch [K11]). Under equilibrium conditions, the maximum drift velocity is v_p (Fig. 8).

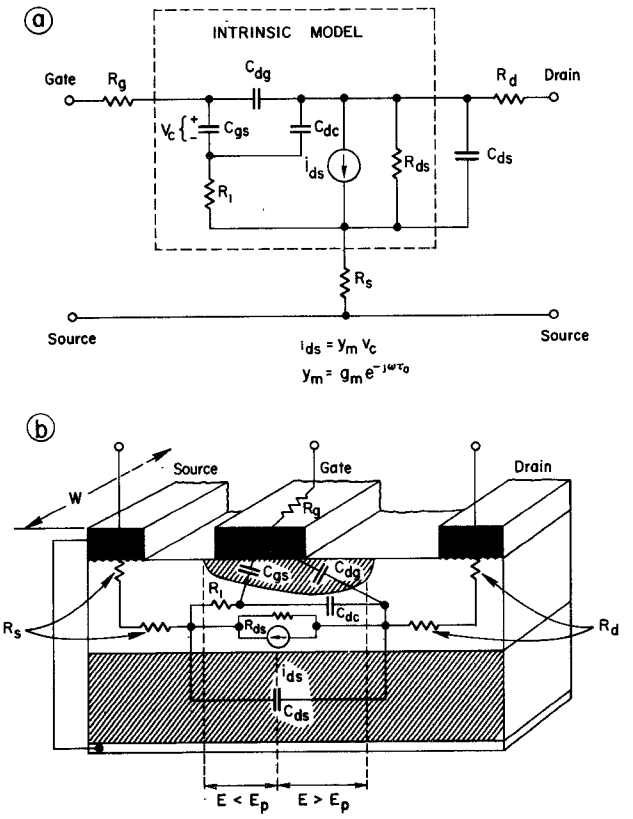

Fig. 11. (a) Is the equivalent circuit of a MESFET. Typical element values are listed in Table III. (b) Shows the physical origin of the circuit elements.

peak equilibrium velocity v_p, and the relaxation to the equilibrium condition, after traveling over a 0.6-μm path length [K11], is shown in Fig. 10. The effect is only noticeable in MESFET's with less than 3-μm gate length [K12], [K13]. The overshoot shortens the electron transit time through the high-field region and shifts the accumulation layer into the gap between gate and drain [K14].

C. Small-Signal Equivalent Circuit

An RF equivalent circuit of the MESFET should model the channel as a distributed RC network. However, a simple lumped-element circuit is capable of describing the FET's s-parameters accurately up to 12 GHz [C1], [C5], [L1]–[L4]. The equivalent circuit for operation in the saturated current region in common-source configuration is shown in Fig. 11(a). The location of the elements in the FET structure is illustrated in Fig. 11(b). In the intrinsic FET model, the elements ($C_{dg} + C_{gs}$) represent the total gate-to-channel capacitance; C_{dc} models the capacitance of the dipole layer; R_i and R_{ds} show the effects of the channel resistance; and i_{ds} defines the voltage-controlled current source. The transadmittance y_m relates i_{ds} to the voltage across C_{gs}. Up to 12 GHz, y_m is characterized by a frequency-independent magnitude, the transconductance g_m, and by a phase delay τ_0, reflecting the carrier transit time in the channel section where $E > E_p$. The extrinsic (parasitic) elements are: R_s the source resistance, R_d the drain resistance, R_g the gate-metal resistance, and C_{ds} the substrate capacitance. Typical element values for a GaAs-MESFET with 1-μm gate length and 500-μm gate width are listed in Table III.

The analysis of the equivalent circuit yields a critical frequency f_k, above which the MESFET is unconditionally stable. f_k can be approximated by[19]

$$f_k \approx \frac{1}{2\pi(\tau_0 + \tau_1 + \tau_2)} \tag{2}$$

[19] Equations (2)–(4) were derived as outlined in [B4].

TABLE III
EQUIVALENT-CIRCUIT PARAMETERS OF A LOW-NOISE GaAs-MESFET WITH A 1-μm × 500-μm GATE
(HP EXPERIMENTAL, $N_D = 1 \times 10^{17}$ cm^{-3})

Intrinsic Elements	Extrinsic Elements
g_m = 53 mmho	C_{ds} = 0.12 pF
τ_o = 5.0 ps	R_g = 2.9 Ω
C_{gs} = 0.62 pF	R_d = 3 Ω
C_{dg} = 0.014 pF	R_s = 2.0 Ω
C_{dc} = 0.02 pF	L_g = 0.05 nH*
R_i = 2.6 Ω	L_d = 0.05 nH*
R_{ds} = 400 Ω	L_s = 0.04 nH*
dc Bias	
V_{DS} = 5 V	
V_{GS} = 0	
I_{DS} = 70 mA	

* Contacting inductances of the test fixture in series with R_g, R_d and R_s, respectively.

where τ_0 is defined in Fig. 11 and

$$\tau_1 = \frac{C_{dg}(2R_g + R_i + R_s)}{\frac{C_{dg}}{C_{gs}} + \frac{R_s}{R_{ds}}} \tag{3}$$

$$\tau_2 = \frac{2}{\frac{g_m}{C_{gs}}\left[\frac{C_{dg}}{C_{gs}} + \frac{R_s}{R_{ds}}\right]} \frac{R_g + R_i + R_s}{R_{ds}}. \tag{4}$$

f_k is 6.1 GHz for the MESFET with the parameters listed in Table III. The MESFET with a complex-conjugate-matched input port becomes unstable with decreasing frequency because a larger fraction of the output voltage is fed back to the input over the $C_{dg} - R_{in}$[20] voltage divider. With decreasing frequency, R_{in} rises as $1/\omega^2$ while the reactance of C_{dg} increases only as $1/\omega$.

Mason's unilateral gain [Q1] is approximately

$$G_u \approx \left(\frac{f_u}{f}\right)^2 \tag{5}$$

where f_u is the maximum frequency of oscillation [B4], [C1]

$$f_u \approx \frac{f_T}{2\sqrt{r_1 + f_T\tau_3}} \tag{6}$$

f_T the frequency at unity current gain

$$f_T \approx \frac{1}{2\pi}\frac{g_m}{C_{gs}} \tag{7}$$

r_1 the input-to-output resistance ratio

$$r_1 = \frac{R_g + R_i + R_s}{R_{ds}} \tag{8}$$

and τ_3 the time constant

$$\tau_3 = 2\pi R_g C_{dg}. \tag{9}$$

Equation (5) shows a gain decreasing with 6 dB/octave as the frequency increases. At f_u, unity gain is reached.[21] To maximize f_u, the frequency f_T and the resistance ratio R_{ds}/R_i must be optimized in the intrinsic MESFET. In addition, the extrinsic resistances R_g and R_s and the feedback capacitance C_{dg} have to be minimized.

D. High-Frequency Limitations

The high-frequency limitations of MESFET's are dependent on device geometry and material parameters. In silicon and GaAs, electrons have a higher mobility than holes. Therefore, only n-channel FET's are used in microwave applications (see Table I). Electrons have six times higher low-field mobility[22] and two times higher maximum drift velocity in GaAs as opposed to silicon. The saturated velocities are about equal in both materials. As a consequence, the realized current-gain bandwidths f_T are about two times higher and the maximum frequencies of oscillation f_u three times higher in GaAs- as opposed to Si-MESFET's [C4], [C9], [C10]. In the device geometry, the most critical parameter is the gate length L. Decreasing the gate length decreases the capacitance C_{gs} and increases the transconductance g_m; consequently, there is an improved current-gain bandwidth f_T. For the short-gate-length microwave MESFET's, f_T is proportional to $1/L$ [J5]. High-speed operation is achieved by shrinking the gate length to the minimum size that can be realized with a given technology. Conventional photolithographic contact or projection-masking limits the smallest features to approximately a 1-μm size. An order of magnitude smaller gate length can be realized with X-ray or electron-beam lithography [X3]. A computer study of submicron Si-MESFET's by Reiser and Wolf [K6] reveals that f_T increases while the output resistance R_{ds} decreases with shrinking gate length. The limit for useful gate reduction is reached when the gate length is about equal to the channel thickness D. To keep $L/D > 1$, the channel thickness has to be decreased together with the gate length. This implies a higher doping level. In practical devices, the highest doping level is about 4×10^{17} cm^{-3} because of breakdown phenomena. The conclusion is that the gate length for Si-MESFET's should be larger than 0.1 μm. This geometry limits the current-gain bandwidth to about 70 GHz [K6]. In GaAs, quantitative high-frequency limitations need to be established. In very short gate devices ($L < 0.2$ μm), the field is above the threshold value E_p over the entire gate length [K9] and electrons are expected to remain in their high-mobility state for the entire flight through the channel [K12], [K13].

E. Principles of Noise Behavior

The noise properties of any linear two-port can be represented by a noiseless two-port with noise-current generators connected across the input and output ports [M1]. This is a physically meaningful way of describing the noise behavior of the intrinsic MESFET (Fig. 12).

The noise-current generator at the output represents the short-circuit channel noise generated in the drain-source path. The mean square of i_{nd} can be expressed by [M2]

$$\overline{i_{nd}^2} = 4kT_0\Delta f g_m P \tag{10}$$

with k the Boltzmann constant, T_0 the lattice temperature, Δf the bandwidth, g_m the transconductance, and P a factor depending on the device geometry and the dc bias. For zero drain voltage, i_{nd} characterizes the thermal noise generated by the drain conductance G_{ds}; i.e., $P = G_{ds}/g_m$. For positive drain voltages, the noise generated in the channel is larger than the thermal noise generated by G_{ds} for the following reasons. First, a thermal noise voltage generated locally in the channel modulates the conductive cross section of the channel and results in an amplified noise voltage at the drain [M2]. Second, the electrons are accelerated in the electric field, then scattered in all directions due to interactions with lattice phonons. Their random drift-velocities and the attributed free-carrier temperature

[20] R_{in} is the effective resistance between gate and source after the conjugate-impedance-matched generator has been connected; i.e.,

$$R_{in} \approx \frac{1}{2\omega^2 C_{gs}^2(R_g + R_i + R_s)}.$$

[21] f_u is 46 GHz for the MESFET of Table III.

[22] The comparison is made for a doping density of 1×10^{17} cm^{-3} [F1], [F8].

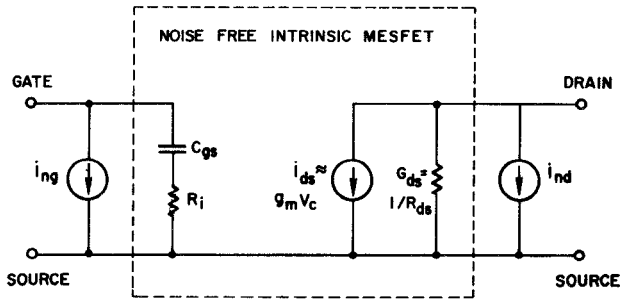

Fig. 12. Equivalent circuit of the (simplified) intrinsic MESFET with noise-current sources at the input and output port.

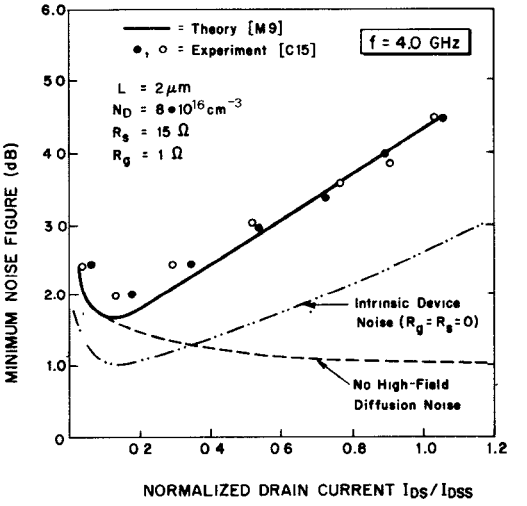

Fig. 13. Theoretical and measured minimum noise figures as a function of normalized drain current for a GaAs-FET with a 2-μm gate. (Courtesy of R. Pucel [C22].)

increase with the applied field to values considerably higher than the lattice temperature (hot-electron noise [M6], [M7]). Third, in GaAs carriers undergo field-dependent transitions from the central valley in the conduction band to satellite valleys and vice versa. A transferred electron experiences an abrupt velocity change. These transitions cause statistical drift-velocity fluctuations and thus generate field-dependent "intervalley-scattering noise" [M8]. Fourth, for large drain voltages, the electrons reach their limiting velocity on the drain side of the channel. In this region, the field has no influence on the carrier drift velocity. Therefore, this channel section cannot be treated as an ohmic conductor. Here, the noise is formulated as high-field diffusion noise[23] [M5], [M9], [M10], and the mean square of the noise current is porportional to the high-field diffusion coefficient in the semiconductor.

A noise voltage, generated locally in the channel, causes a fluctuation in the depletion-layer width. The resulting charge fluctuation in the depletion layer in turn induces a compensating charge variation on the gate electrode. The total induced-gate charge fluctuation is described in Fig. 12 by a noise-current generator i_{ng} at the gate terminal [M3] where

$$\overline{i_{ng}^2} = 4kT_0\Delta f \frac{\omega^2 C_{gs}^2}{g_m} R. \tag{11}$$

C_{gs} is the gate-source capacitance and R a factor depending on the FET geometry and the bias conditions.[24] The two noise currents, i_{nd} and i_{ng}, are caused by the same noise voltages in the channel. Therefore, partial correlation has to be expected.[25] A correlation factor C is defined as [M3]

$$jC = \frac{\overline{i_{ng}^* \cdot i_{nd}}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}} \tag{12}$$

where j is the imaginary unit and the asterisk defines the complex conjugate. The correlation coefficient is purely imaginary because i_{ng} is caused by capacitive coupling of the gate circuit to the noise sources in the drain circuit. The factors P, R, and C in (10)–(12) have been computed versus normalized gate voltage by Baechtold [M8] for GaAs-MESFET's with various channel length-to-height ratios operated at the onset of current saturation. Statz *et al.* [M9] have extended the computation of P, R, and C to large drain voltages taking diffusion noise in the velocity-saturated channel region into account.

Using the model of Fig. 12, the minimum noise figure of the intrinsic MESFET can be expressed by [M7], [M10]

$$F_{\min} = 1 + 2\sqrt{PR(1-C^2)}\frac{f}{f_T} + 2g_m R_i P\left(1 - C\sqrt{\frac{P}{R}}\right)\left(\frac{f}{f_T}\right)^2. \tag{13}$$

Low-noise MESFET's are normally operated at frequencies below f_T in order to yield sufficient gain. In this case, the linear frequency term in (13) is dominant. Short-gate MESFET's can exhibit very low noise figures for the following reasons. For an optimized drain current ($I_{DS}/I_{DSS} \approx 0.15$), the diffusion-noise contribution is small (Fig. 13), f_T is close to its maximum value [W3], and the correlation coefficient approaches unity ($C \approx 0.9$ [M9]). Substantial noise cancellation occurs at the drain which is expressed by the factor $(1 - C^2)$ in (13). The amplified input-noise current (αi_{ng}) destructively interferes with the correlated i_{nd} if the MESFET's gain and transmission phase are properly adjusted with an optimized input termination

$$\overline{|\alpha i_{ng} + i_{nd}|^2} \ll \overline{|\alpha i_{ng}|^2} + \overline{|i_{nd}|^2}. \tag{14}$$

In a practical MESFET, the parasitic resistances R_g and R_s, shown in Fig. 11, decrease the effectiveness of this noise cancellation [C22], [M9] and, in addition, they generate thermal noise themselves. A comparison between theoretical and experimental noise figures versus drain current is shown in Fig. 13. The increase of $F_{\min}$ with drain current is caused by the diffusion noise in the velocity-saturated

[23] The diffusion-noise theory is also valid at low fields and is a more general formulation than Johnson's formula for the thermal noise of a conductance [M5].

[24] For zero drain voltage, i_{ng} is the thermal noise of the input conductance $g_{11}(g_{11} \approx \omega^2 C_{gs}^2 R_i)$, and R is equal to the product $g_m R_i$.

[25] Complete correlation results for a channel with uniform conductive cross section (e.g., for zero drain voltage).

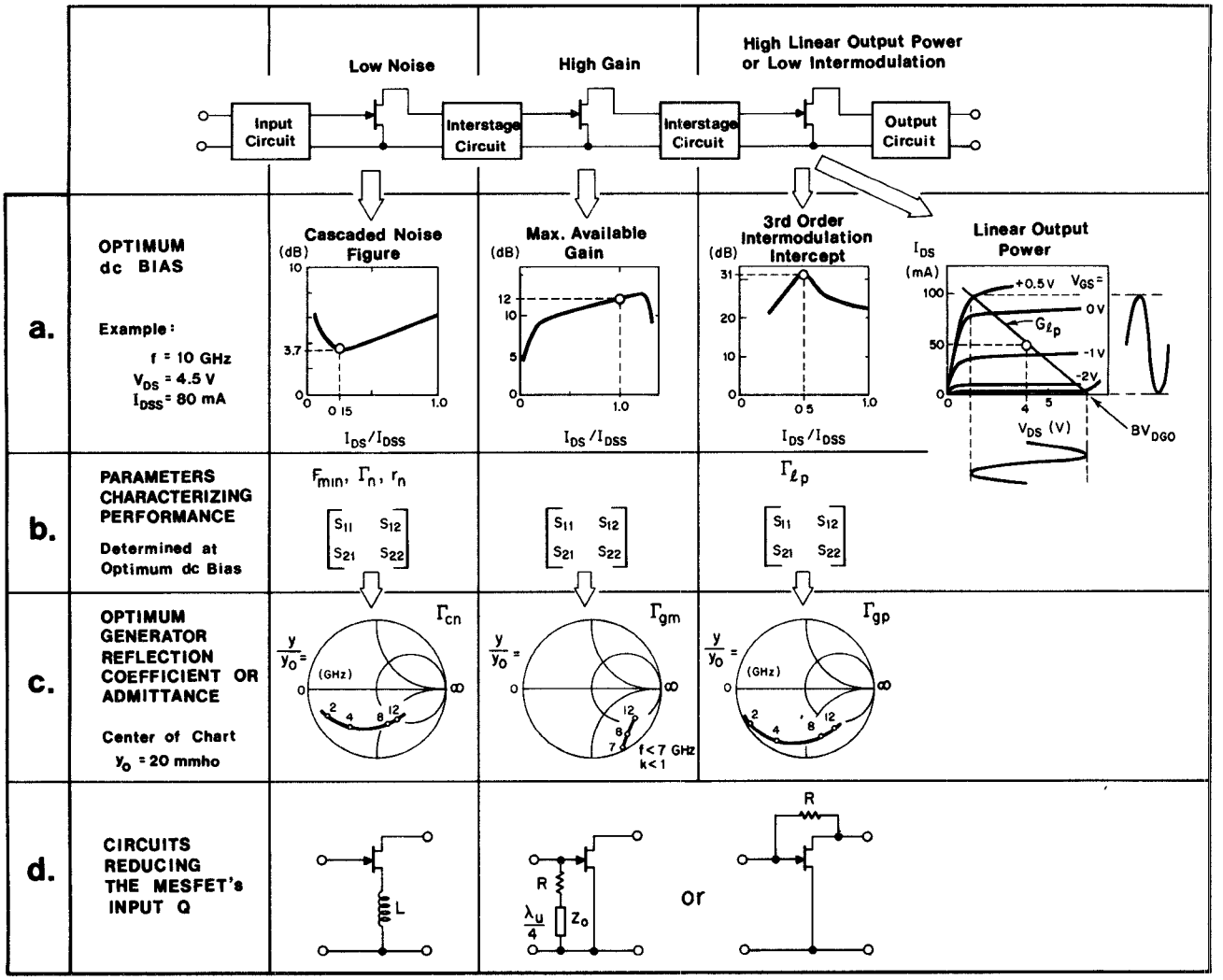

Fig. 14. The figure shows the key parameters in operating a MESFET in either a low-noise front stage, a high-gain stage, or a linear-power stage. (a) Illustrates the FET characteristics leading to the optimum dc bias. (b) Lists the parameters characterizing the performance (e.g., as computer input for CAD). (c) Shows optimum generator reflection coefficient to be synthesized by the circuits. The example is based on an HP MESFET with 1-μm gate length and 500-μm gate width. (d) Shows circuits to reduce the MESFET's input Q or to stabilize the transistor at low frequencies.

region [M9]. The noise-figure rise for small drain currents is caused by the rapid decrease of g_m and consequently of f_T. Also shown is the computed noise figure of the intrinsic MESFET.

IV. MESFET Amplifiers

In this section, basic concepts in the design of low-noise and linear medium-power MESFET amplifiers are reviewed.[26] The optimum dc bias, the parameters for device characterization, and the optimum generator admittance are discussed. Principles for network synthesis are described. Finally, performance characteristics of low-noise MESFET amplifiers are presented. As an example, an amplifier with a low-noise front stage, a high-gain stage, and a power-output stage is considered (Fig. 14). The amplifier shall be designed for low noise figure, flat gain, and high linear output-power capability across a specified band.

A. Optimized Operating Conditions for the MESFET's

The MESFET in the first-amplifier stage has to be operated at the dc bias yielding the lowest cascaded noise figure[27]

$$F_c = \frac{FG - 1}{G - 1} \tag{15}$$

where F_c is the noise figure of an infinite number of cascaded stages each having a noise figure F and gain G. F_c is nearly independent of the drain voltage as long as $V_{DS} > V_{D_{sat}}$; however, strongly dependent on the drain current [C15], [M7], [M9]. Typically, F_c reaches a minimum at 0.1–0.2I_{DSS} [C15], [D4], [M9] where I_{DSS} is the

[26] The reader is also referred to recent review papers on solid-state microwave amplifiers by Cuccia [O1], Magarshack [O2], and Osbrink *et al.* [O3].

[27] The term "noise measure," M, proposed by Haus and Adler [N1], is omitted here. Instead, the "cascaded noise figure," F_c is adopted. The relationship between F_c and M is $F_c = 1 + M$.

saturated drain current at zero gate voltage [Figs. 13 and 14(a)]. The drain current is adjusted to this optimum value with the gate bias. In this operating point, the MESFET's noise behavior is characterized by 1) the minimum noise figure $F_{\min}$; 2) the reflection coefficient of the generator Γ_n, which produces $F_{\min}$; and 3) a dimensionless coefficient r_n [N2]–[N9]. For an arbitrary generator reflection coefficient Γ_g, the noise figure is then determined by

$$F = F_{\min} + 4r_n \frac{|\Gamma_g - \Gamma_n|^2}{(1 - |\Gamma_g|^2)|1 + \Gamma_n|^2}. \quad (16)$$

If the s-parameters are known, all parameters of interest can be computed. These are, e.g., the optimum generator reflection coefficient for lowest cascaded noise figure Γ_{cn} [N3], [N9], the optimum load reflection coefficient, the associated transistor gain (17), etc. Γ_{cn} is in general different from the reflection coefficient for maximum gain Γ_{gm} [Fig. 14(c)]. A combination of lossless parallel and series feedback is capable of making Γ_{cn} and Γ_{gm} identical without changing F_c[28] [N10]–[N14].

The MESFET in the second stage is operated with maximum small-signal gain [Fig. 14(a)]. This condition is obtained at approximately zero gate voltage ($I_{DS} \approx I_{DSS}$), where f_T reaches a maximum, and at a drain voltage that maximizes the output resistance and the resistance ratio $1/r_1$ in (8). The small-signal behavior is fully characterized with the four s-parameters [Q3]. The transducer gain [29] for any generator and load reflection coefficients, Γ_g and Γ_l, respectively, is [Q4]

$$G = \frac{|s_{21}|^2(1 - |\Gamma_g|^2)(1 - |\Gamma_l|^2)}{|(1 - s_{11}\Gamma_g)(1 - s_{22}\Gamma_l) - s_{12}s_{21}\Gamma_g\Gamma_l|^2}. \quad (17)$$

The s-parameters determine also Rollett's [Q2] stability factor k

$$k = \frac{1 + |s_{11}s_{22} - s_{12}s_{21}|^2 - |s_{11}|^2 - |s_{22}|^2}{2|s_{12}s_{21}|}. \quad (18)$$

If k is larger than unity,[30] an optimum combination of Γ_{gm} and Γ_{lm} simultaneously image-matches the two MESFET ports and maximizes the gain [Q4]. If k is smaller than unity, the MESFET is only conditionally stable. In this case, the terminations Γ_g and Γ_l must be carefully chosen to operate the transistor in a stable range [Q4], [Q5] or the resistive stabilization networks described below must be applied. Frequently, $k \gg 1$ and $|s_{12}|$ are small enough for the MESFET to be treated as a unilateral two-port ($s_{12} = 0$; $k = \infty$). In this case, the optimum generator and load terminations are

$$\Gamma_{gm} = s_{11}^* \qquad \Gamma_{lm} = s_{22}^* \quad (19)$$

and the maximum available gain obtained from (17) is

$$G_{\max} = \frac{|s_{21}|^2}{(1 - |s_{11}|^2)(1 - |s_{22}|^2)}. \quad (20)$$

The asterisk in (19) defines the complex conjugate of the s-parameters.

The MESFET in the output stage is intended to operate as a linear (Class A) amplifier. The design objectives can be either lowest intermodulation distortion [P1]–[P3], largest added RF power [Q6], or largest linear output power [T1]. In the last case, the dc bias is graphically determined from the static drain-current versus drain-voltage characteristic. The bias and load conductance line are chosen to maximize the product of linear voltage and current swing [Fig. 14(a)]. The limitations are determined by the maximum dc power dissipation, the drain-to-gate breakdown voltage BV_{DGO}, and the positive gate bias ($V_{GS} \approx 0.5$ V) above which appreciable gate current flows. The optimum load conductance is typically much larger than the MESFET's output conductance. Consequently, the MESFET is not matched to the load and does not deliver maximum gain. However, the large load conductance shunting the MESFET's nonlinear output admittance reduces intermodulation distortion.[31] The optimum load conductance and susceptance determine the optimum reflection coefficient of the load Γ_{lp}. The generator reflection coefficient that provides a complex-conjugate match at the input is then

$$\Gamma_{gp} = \left[s_{11} + \frac{s_{12}s_{21}\Gamma_{lp}}{1 - s_{22}\Gamma_{lp}}\right]^* \quad (21)$$

and the associated gain is determined from (17).

Optimum generator reflection coefficients for low noise, high gain, and high linear-power operation are shown in Fig. 14(c). The plotted data are typical for an unpackaged small-signal GaAs-MESFET with 1-μm gate length and 500-μm gate width. At low frequencies, the FET has a high-Q input admittance and wide-band matching is difficult. Simple circuits that lower the Q value are illustrated in Fig. 14(d). A series-feedback inductance between source and ground increases the input series resistance, decreases the input reactance, and leaves F_c unchanged. A resistor in-series with a short-circuited shunt stub, connected between gate and source, lowers the Q and stabilizes the FET at the low-frequency end of the band [T1]. If the shunt stub is a quarter-wavelength long at the upper band edge, the circuit does not load the FET input and does not decrease the gain at this frequency. Also, a parallel feedback resistance has been proposed for stabilization and input Q lowering [Q7].

B. Amplifier Network Synthesis

The input-matching network transforms the 50-Ω generator impedance to the optimum impedance with

[28] The MESFET's noise figure F and gain G change, but the cascaded noise figure F_c remains invariant.

[29] The transducer gain is defined as the power delivered to the load divided by the available power from the generator.

[30] i.e., the MESFET is operated above the critical frequency f_k discussed in Section III.

[31] If low third-order intermodulation is desired [Fig. 14(a)], a drain current is chosen that minimizes the distortion from the nonlinear transconductance and input capacitance [P3].

reflection coefficient Γ_{cn}. The transformed impedance versus frequency must have a negative-reactance slope, $dX/df < 0$. For narrow-band amplifiers, the circuit is derived from a simple graphical design using the Smith chart [L4], [N3], [Q9]–[Q12]. For moderate-bandwidth MESFET amplifiers, impedance-matching bandpass networks with quarter-wave resonators have been applied successfully [Q13]. These networks are derived from low-pass filter prototypes; the circuit topology is well defined, and the element values are optimized by simple computations. The design procedures treat the MESFET as a unilateral device ($s_{12} = 0$). For more accurate optimizations and for large bandwidths, computer-aided design procedures are used in which the MESFET is characterized by all noise- and s-parameters [Q14]–[Q19]. In general, a particular circuit topology is chosen by the designer. The values of the circuit elements are then optimized by the computer. The optimization routine searches in a systematic way for the global minimum of an error function E defined as

$$E = \sum_{f_1}^{f_n} [\text{calculated } H(f) - \text{required } H(f)]^2 \quad (22)$$

where f is the frequency and H is a performance function defined as a weighted sum of gain, noise figure, reflection coefficients, etc. The matching networks are normally built as microstrip circuits. A monolithic amplifier stage, combining lumped matching elements with the MESFET on a single GaAs chip, has also been reported [B1], [R13]. The amplifier modules exhibit very broad-band performance (6–12.4 GHz).

In the interstage networks, the insertion loss versus frequency response has to compensate the MESFET's gain slope [Fig. 15(a)] to achieve a flat amplifier gain. Generally, this is done by matching the output of the preceding FET to the input of the following transistor at the upper band edge and providing an increasing mismatch with decreasing frequency [Fig. 15(b)]. Analytical methods have been developed for the synthesis of reactive networks yielding the desired insertion loss versus frequency characteristic [Q20]–[Q24]. Since the gain slope is provided by reactive mismatch, high standing waves result between the stages at the lower band end. The high voltages generated in the standing waves enhance feedback in the FET's and the large reactance versus frequency slopes of the networks cause high group-delay variations. These problems can be avoided with dissipative coupling networks [Q13], [Q25], [Q26] which provide a lossless impedance match at the highest frequency in the band and introduce increasing resistive loss (attenuation) with decreasing frequency [Fig. 15(c)]. The amount of gain compensation has to be individually chosen for each interstage network to achieve lowest amplifier noise figure across the entire band [Q25] and to prevent premature power saturation in the driver stage [Q26].

MESFET amplifiers are built with balanced and unbalanced circuits. Balanced amplifiers consist of a pair of amplifiers or single-tuned stages whose inputs are connected to the

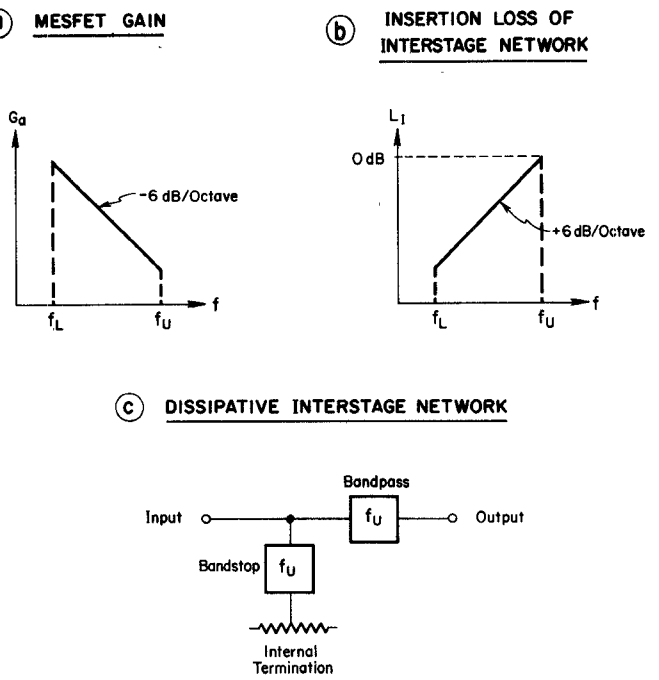

Fig. 15. For a flat amplifier gain, the MESFET's gain versus frequency slope (a) has to be compensated by an inverse slope in the interstage network's insertion loss (b). The insertion-loss characteristic can be obtained with reactive mismatch in an L–C network or with frequency-dependent attenuation in a diplexer resulting in dissipation of the excess power in an internal termination (c).

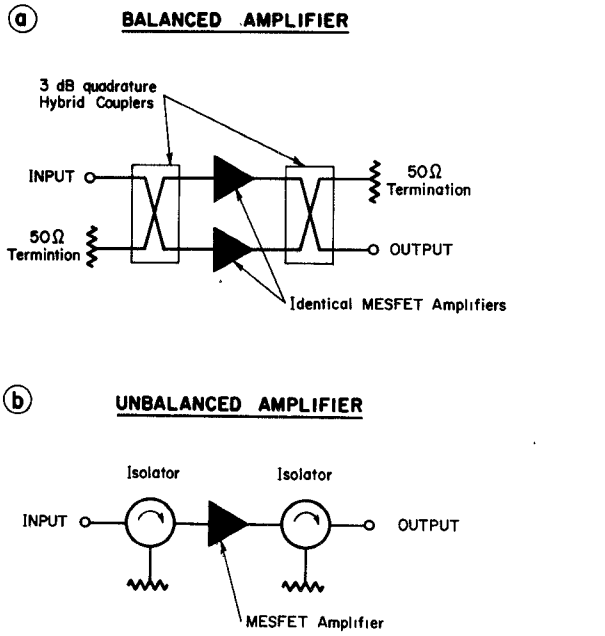

Fig. 16. MESFET amplifiers are built in balanced form with 3-dB hybrid couplers at the input and output of each stage or as an unbalanced chain of stages with isolators on both amplifier ports.

conjugate ports of a 3-dB hybrid coupler and whose outputs are similarly connected to another 3-dB coupler [Fig. 16(a)] [Q27]. The signal applied at the input port of the first coupler splits into two equal parts and is fed to the two amplifiers. The amplified signals from the two amplifier outputs recombine in the second coupler and emerge at one of the coupler's output ports. The advantages of the balanced

amplifier over an unbalanced amplifier are improvement in: 1) input and output impedance matching in an amplifier optimized for noise figure or output power, 2) short- and open-circuit stability, 3) phase linearity, 4) gain compression, 5) intermodulation characteristics, and 6) reduced sensitivity to transistor impedance variations, provided the MESFET's are selected in similar pairs. Unbalanced amplifiers, on the other hand, need only half as many MESFET's, matching networks, and dc power. In general, isolators are required at the input and output of broad-band unbalanced MESFET amplifiers to meet low VSWR specifications and to make the noise figure independent of the source admittance [Fig. 16(b)]. 3-dB hybrid couplers are also used for power combining [Q28] as shown in Fig. 17.

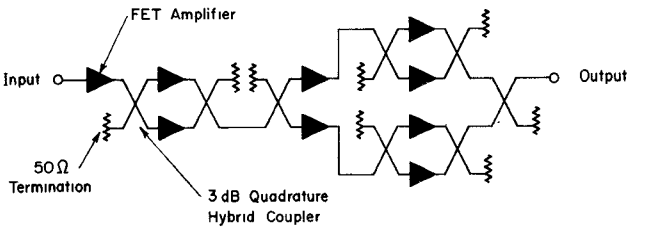

Fig. 17. In transistor power amplifiers, 3-dB hybrid couplers are also used as power combiners (after S. Lazar [Q28]).

C. MESFET Amplifier Performance

Various small-signal FET amplifiers have been described in the literature [C14], [D6], [G3], [P3], [Q7], [Q13], [Q22], [R1]–[R15]. Most are low-noise designs. Noise figures of laboratory prototypes are plotted versus frequency in Fig. 18. The solid lines represent narrow-band amplifiers. Lowest noise figures are 2.2 dB at 4 GHz, 3.6 dB at 8 GHz, and 5.0 dB at 12 GHz. The single data points (circles, squares, etc.) show noise figures of the 1-μm MESFET's used in the first amplifier stages. The data points lie about 1.0 dB below the amplifier noise figures. The noise-figure difference is caused by the insertion loss of the input circuit and by the noise contribution of the following stages. The noise figures of wide-band amplifiers, plotted with dashed lines, are typically 1.0–1.5 dB higher than the narrow-band circuits. At room temperature, thermal-noise sources dominate the noise performance of GaAs MESFET's in microwave amplifiers [M8], [M9]. By cooling the amplifier, a significant noise reduction can be obtained [S1]–[S6]. 1.6-dB noise figure (i.e., 130 K input noise temperature) was measured at 60 K for a 12-GHz amplifier [S5], [S6].

Octave-band MESFET amplifiers covering the 4.0–8.0-GHz frequency range have been built in balanced form [C14], [R5], [R6], [T3]. Typically, a three-stage small-signal amplifier has 24-dB gain, $\pm$0.7-dB gain variation, 1.8:1 maximum VSWR at the input and output port, +13-dBm output power for 1-dB gain compression, and +20-dBm third-order intermodulation intercept [R16], [R17]. In the 8.0–12.0-GHz band, a three-stage unbalanced amplifier without isolators exhibits 20 $\pm$1.3-dB gain, 2.5:1 maximum VSWR, +13-dBm output power, and +26-dBm intermodulation intercept [Q13]. Less gain variation, e.g., 28.5 $\pm$0.5 dB, can be obtained with a balanced design [R15].

A few medium-power amplifiers have been reported [T1]–[T6]. At 6 GHz, a four-stage amplifier with 26-dB gain and 1-W output power,[32] using a single MESFET chip in the output stage, has been built [T2]. More common are balanced output stages which combine the output power of two transistors [T1], [T3], [T6]. Also, wide-band medium-power amplifiers have been designed [T1], [T3],

[32] Measured at 1-dB gain compression.

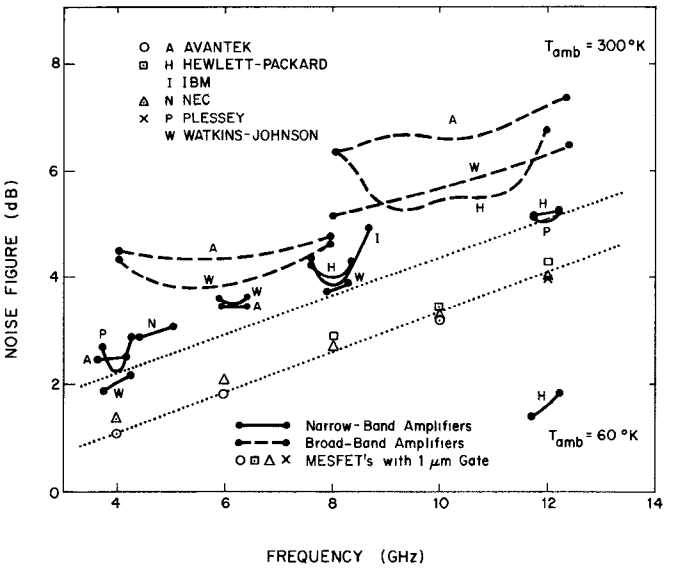

Fig. 18. This noise figure versus frequency graph summarizes performance of experimental MESFET amplifiers. The solid lines represent narrow-band amplifiers, and the single data points show noise figures of the 1-μm MESFET's used in the first stages. The broken lines illustrate the noise performance of wide-band amplifiers.

and one covers the 2–6-GHz band [T1]. In this frequency range, MESFET's with 1-μm gate length have a high-Q input impedance, and matching circuits with resistive components, illustrated in Fig. 14(d), must be used.

V. Other Applications

So far, comparatively little effort has been spent on the development of GaAs-MESFET oscillators [U1]–[U8]. This application should prove to be of interest since MESFET's combine the advantages of low bias voltage (< 10 V), relatively low noise measure (< 23 dB),[33] and high efficiency (> 15 percent at 10 GHz [U2]). Also GaAs-MESFET mixers [V1]–[V5] are expected to receive more attention in the near future. Good noise performance (F = 7.4 dB)[34] and large dynamic range (third-order intermodulation intercept = +18 dBm)[34] can be achieved with conversion gain (G = 6-dB)[34] [V3]. Another application is the use

[33] This oscillator noise measure is measured at 1-MHz separation from the X-band carrier [U3]. This noise measure is high in comparison to amplifier noise figures because of upconverted $1/f$ noise. Reduction of traps at the active-layer surface and at the substrate interface is expected to improve the low-frequency noise performance of GaAs-MESFET's in the near future.

[34] Measured at 8 GHz with a balanced MESFET mixer.

of Si-MESFET's [W1], [W2] and GaAs-MESFET's [W3]–[W7] or GaAs-JFET's [W8], [W9] in high-speed digital circuits. Monolithic integrated-logic gates with 100-ps signal-propagation delay (fanout 2) and 4-pJ speed-power product have been built using 1-μm GaAs-MESFET's [W3], [W4]. This is less than half the propagation delay measured on highest speed bipolar logic [W10], [W11]. In addition, the feasibility for medium-scale integration of these GaAs circuits has been demonstrated [W4].

VI. Conclusions and Outlook

GaAs-FET's are capable of low-noise amplification, high-efficiency power amplification and generation, high-speed modulation, and logic. Since these are areas of major microwave-system needs, substantial efforts in device and application developments are anticipated. In the near future, rapid advances are expected in the areas of 1) FET reliability, 2) device fabrication with high yield, uniform and reproducible unit-to-unit parameters by means of ion implantation, and electron-beam lithography, and 3) higher power capability and efficiency due to improved device structures with better heat sinking, thermally stable ohmic contacts, and more burn-out-resistant gates. Looking further ahead, a strong trend toward monolithic integration for digital, analog, and hybrid applications is now apparent. The monolithic approach is attractive because MESFET's fabricated on the same active layer can be used as switches, logic gates with active loads, impedance transformers, amplifiers, oscillators, and mixers; and the devices can be supported, isolated, and interconnected with low parasitic capacitances on the semi-insulating substrate. Monolithic integration is required to handle the complexity of tasks and to serve high-volume low-cast markets. Integrated high-speed logic will be needed in digital communications with gigabit-per-second data rates [W12]–[W14], in multi-phase-shift-keyed modulation and demodulation, time multiplexing, frequency division, counting, frequency synthesis, and waveform synthesis. A need is foreseen for microwave analog and hybrid circuits, on a single chip, such as 1) combinations of a preamplifier, mixer, local oscillator, and IF amplifier, 2) wide-band signal and operational amplifiers, 3) sample and hold circuits, and 4) high-speed D/A and A/D converters. Advances in III–V materials preparation and in submicron device processing will make microwave monolithic circuits with FET's a reality.

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Submicron Single-Gate and Dual-Gate GaAs MESFET's with Improved Low Noise and High Gain Performance

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Abstract—**Microwave performance of single-gate and dual-gate GaAs MESFET's with submicron gate structure is described. Design consideration and device technologies are also discussed. The performance of these GaAs MESFET's exceeds previous performance with regard to lower noise and higher gain up to *X* band: 2.9-dB noise figure (NF) and 10.0-dB associated gain at 12 GHz for a 0.5-μm single-gate MESFET, and 3.9-dB NF and 13.2-dB associated gain at the same frequency for a dual-gate MESFET with two 1-μm gates.**

I. Introduction

SINGLE-GATE [1], [2] and dual-gate [3], [4] GaAs MESFET's have been extensively developed, showing low noise and high gain properties at microwave frequencies. Improvements have been successfully attained mainly due to gate length reduction. As a result of advanced photolithography 0.5-μm-gate MESFET's with 4–5-dB noise figures (NF) at 12 GHz have been realized [2].

However, calculations on the NF [5] revealed that the observed NF values were still large compared with the theoretical ones. The discrepancy is considered to be partly due to the degraded crystal quality in the epitaxial film near the substrate and partly due to the effects of parasitic resistances. This suggests that refinement of epitaxial growth and metallization technologies is more urgently required than further gate length reduction to produce decreased NF.

The purpose of this work is to realize improved GaAs MESFET's based on refinement of these technologies. Details of epitaxial wafer preparation and of contact metallization processes are described in Section II. Design consideration and fabrication of single-gate (0.5-μm-gate and 1.0-μm-gate) and dual-gate (1-μm–1-μm-gate) MESFET's are described in Section III. MESFET microwave performance is described in Section IV.

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II. Device Technology Refinement

A. Epitaxial Wafer Preparation

The gallium arsenide wafer used in this work consists of a thin and highly doped n-type active layer, a high-resistivity buffer layer, and a semi-insulating substrate. Both buffer and active layers were successively grown on the substrate in the modified $Ga/AsCl_3/H_2$ reaction system [6].

1) Buffer Layer: At the dc bias point, where minimum NF is observed, carriers are confined in an approximately 100-Å-wide n-type epitaxial region adjacent to the substrate. Thus crystal properties, such as electron mobility and impurity concentration in this region, have the dominant effect on MESFET performance.

Electron mobility degradation in the region near the